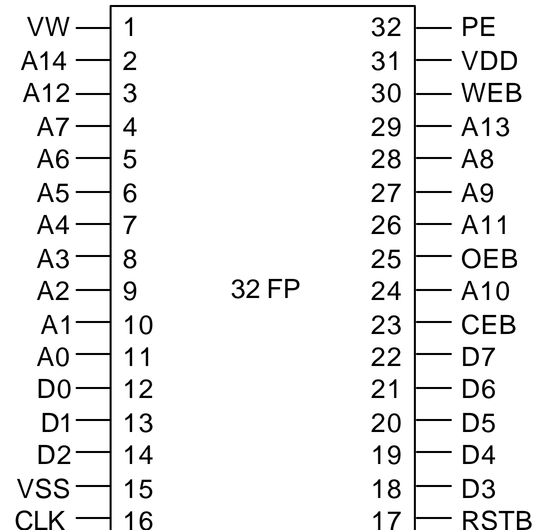
W28C256
Radiation Hardened 32K x 8 CMOS EEPROM

Northrop Grumman Corporation
January 2001

Features

- **1.25 Micrometer Radiation Hardened CMOS on Epi**
  - Total Dose up to 300 Krad (Si)
  - Transient Logic Upset >5E7 Rad(Si)/sec
  - Memory Data Loss >1E12 Rad(Si)/sec
- **Single Event Upsets**
  - SEU During READ LETth = 60 $MeV/mg/cm^2$
  - SEU in Address/Data Latches, LETth = 35 $MeV/mg/cm^2$
  - Permanent SEU damage (During Write Only), Atomic Number ≥ Kr
- No Latchup
- Compatible with commercial EEPROMs
- JEDEC pin compatible in center 28 pins
- Full military operating temperature range, screened to specific test methods for commercial, Class B, or modified Hi Rel.



PINOUT
(Top View)

Supports these commercial features:

- Self-Timed Programming
- Combined Erase/Write
- Auto Program Start
- +5V only read operation
- Asynchronous Addressing
- 64 Word Page
- Data Polling

Introduction

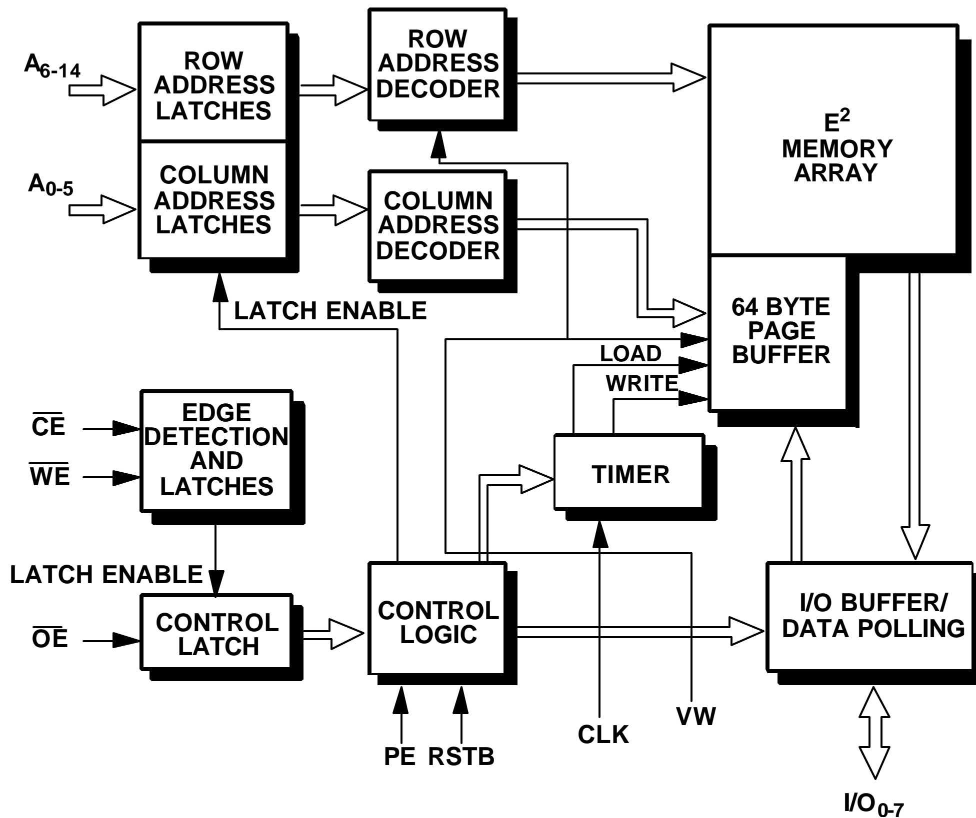
The W28C256 is a 32K x 8 radiation hardened EEPROM designed by Sandia National Laboratories, Albuquerque NM, and manufactured by the Northrop Grumman Advanced Technology Center, Baltimore MD, using nonvolatile memory technology transferred from Sandia. It is built using a mature dual well CMOS process using N on N+ epitaxial silicon and a two layer interconnect system.

Caution: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. handling procedures.

Absolute Maximum Ratings

SYMBOL	PARAMETER	VALUE	UNITS
TSTG	Storage Temperature	-65 TO +150*	°C
TA	Operating Temperature	-55 TO +125	°C
VDDR	Power Supply During Read	6	V
VW	External Write Voltage With Respect To VDD	-10.5	V
VTERM	Terminal Voltage With Respect To Ground	6.5	V
TL	Lead Temperature (Soldering 10 sec)	300	°C

* See data retention discussion on page 4.



DC Operating Characteristics
T_A = -55° to + 125°C, VDD = 5V ±5%, unless otherwise specified

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
IDDS	Static I Read		10	mA	Read Mode, DC
IDDR	Active I Read		17	mA	Read Mode, 2 MHz
IDDW	Active I Write		2	mA	Write Mode
IW1	Inactive I Write	-25		uA	Standby or Read (Note 1)
IDDSB	Standby I		1.5	mA	
IIH	Input I High		1	uA	
IIL	Input I Low		1	uA	
IOH	Output I High		3	mA	VOH = 4.25V
IOL	Output I Low	-3		mA	VOL = 0.5 V
VIL	Input V Low	-0.5	0.95	V	
VIH	Input V High	3.8	VDD +0.5	V	
VOH	Output V High	4.25		V	VDD = 4.75 VW = -4.75 VIH = 3.8 VIL = 0.95 IOL = -3 mA (Note 2)
VOL	Output V Low		0.5	V	VDD = 4.75 VW = -4.75 VIH = 3.8 VIL = 0.95 IOH = 3 mA (Note 2)
IOZL	Tristate Leakage Low	-10		uA	
IOZH	Tristate Leakage High		10	uA	

Notes:
1. Tested but not recorded
2. Verified by functional testing

Mode Selection

MODE	CEB	OEB	WEB	PE	A(12:0)	I/O
Read	VIL	VIL	VIH	VIL	ADDR	DOUT
Standby	VIH	X	X	VIL	XXX	HI Z
Write	VIL	VIH	VIL	VIL	ADDR	DIN
Write Inhibit	X X	X VIL	VIH X	VIL VIL	XXX XXX	HI Z/DOUT HI Z/DOUT

Pin Description Addresses (A0-A14)
The address inputs select which byte will be accessed during a read or write operation. A0-A5 are the column or byte addresses and A6-A14 are the row or page addresses.

Chip Enable (CEB)
This input must be LOW during read and write operations. After a programming operation has been initiated, the chip may be deselected. When the part is deselected, the outputs are tristated.

Output Enable (OEB)
This input controls the output buffers. When HIGH the outputs are tristated and when LOW the outputs are driven to the correct CMOS levels.

Data (D0-D7)
Data is written to or read from the part using these pins.

Write Enable (WEB)
This input controls the writing of data. When low, write is enabled.

Clock Input (CLK)
The clock input is used to time the programming functions. The nominal value for a 10 ms write cycle is 2 MHz. The clock is not required for read operations. The clock waveform has no critical timing with respect to other input or output signals.

Reset Input (RSTB)

The reset input is active LOW and is used to prevent programming during power transitions or during high transient radiation doses. This signal should be held low during power up and power down.

Write Voltage (VW)

This -5V±5% supply pin is used to provide the internal programming voltage. This pin may be tied to OV during read operations. During power up VDD must come up first, then Vw; and during power down Vw must go off first, then VDD.

Program Enable Input (PE)

This pin is used for testing and validation purposes to gain more control over internal chip operation. Normal operation requires this pin to be tied LOW.

Data Polling

The programming time for the W28C256 is controlled by an internal counter and the externally supplied clock input. The nominal timing is for a 10 ms programming time with a 2 MHz clock input. The Data Polling mode can be used to verify the completion of programming. If a read is performed on any address while the part is still being programmed, the ones complement of the last byte written will be presented at the outputs. After programming has completed, a read of the last address written will result in the correct data being presented at the outputs. To monitor for completion of programming the user can read the last address written until the correct data is read.

Data Retention

The W28C256 EEPROM is based on SONOS nonvolatile memory technology. SONOS is an acronym for Silicon-Oxide-Nitride-Oxide-Silicon. The memory device is a silicon gate N-channel MOS transistor with a specially processed gate dielectric consisting of a tunnelling oxide, a silicon nitride layer, and a capping oxide. SONOS technology is used in preference to conventional floating gate technology because of its superior reliability and radiation hardness. The SONOS memory effect relies on charge storage within the silicon nitride film, with the silicon dioxide above and below it acting as energy barriers to the loss of charge. The charge is injected by tunnelling through the tunnelling oxide.

The charge deposited in the SONOS dielectric does decay slowly with time, but when written under the specified conditions and stored within the specified limits, data is indeed permanent for most purposes. Data loss is accelerated by both temperature and radiation, and is also affected by the number of write cycles the device has seen previously.

Write cycles must, however, be accumulated in the tens of thousands before any effect on retention is seen. When written using a 2 MHz external clock, nonvolatile data storage is guaranteed through 100 K Rad (Si), without rewriting, at the specified temperature range. In satellite applications, this normally corresponds to many years of service.

For operation beyond 100 K Rad (Si), data should be written after every 100 K Rad of accumulated total dose. In addition to the memory devices themselves, a key feature of this device is the radiation hardened peripheral circuitry. This circuitry remains virtually unaffected by radiation effects within the limits specified over the full range of device operation.

For proper retention and reliability, the memory devices require careful control of the clear/write conditions. This applies particularly to the control of the clear/write voltage. The clear/write time (pulsewidth) is also important.

Consequently, both a Clock pin and a Vwrite pin are provided. With a nominal 2 MHz clock and Vw = -5V±5%, this device emulates commercial EEPROMs. Under these conditions, data retention is guaranteed for a minimum of 10 years. The external clock is required for write mode only, read mode is asynchronous and no clock is required.

Temperature	Retention (Years)	Cycles	Total Dose K Rad (Si)
-55 to 80°C	10	10,000	0 to 50
-55 to 80°C	10*	1,000	50 to 100
Rewriting after 100 K Rads results in another 10 years of retention up to a max total dose specified			

AC Operating Characteristics (Write Operations)
T_A = -55 to + 125°C, VDD = 5V ±5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	MAX		
f_C	Clock Frequency	1	2	MHz	Write Mode (Note 1)
t_{WC}	Write Cycle Time		10	ms	fc = 2 MHz (Note 1)
t_{AS}	Address Setup Time	0		ns	
t_{AH}	Address Hold Time	150		ns	
t_{CS}	Write Setup Time	0		ns	
t_{CH}	Write Hold Time	0		ns	
t_{CW}	CEB Pulse Width	150		ns	
t_{OES}	OEB High Setup Time	10		ns	
t_{OEH}	OEB High Hold Time	10		ns	
t_{WP}	WEB Pulse Width	150		ns	
t_{DS}	Data Setup Time	0		ns	
t_{DH}	Data Hold Time	60		ns	
t_{BLC}	Byte Load Cycle	0.2	250	µs	fc = 2 MHz
t_{LP}	Last Byte Loaded to Data Polling Output	300		µs	fc = 2 MHz

Note:

1. Verified by functional testing.

Write Cycle

Note: All or a portion of the 64 byte page may be loaded prior to writing, but the entire page is always written with the contents of the data latches. Single byte data modification is not supported.

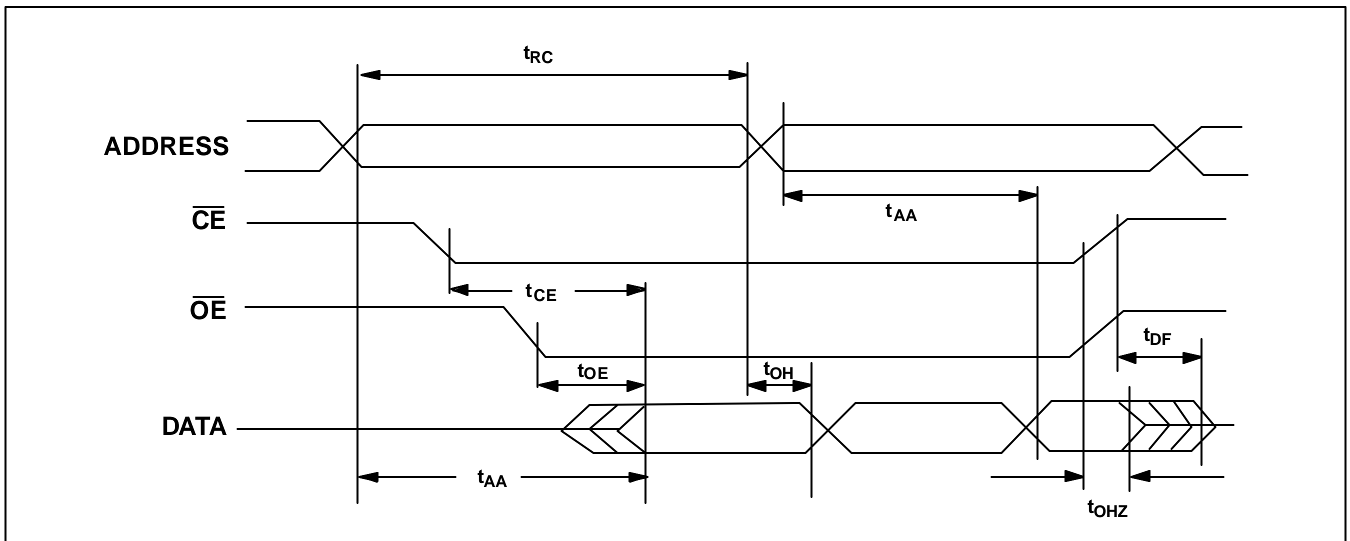
AC Operating Characteristics (Read Operations)
T_A = -55 to 125°C, VDD = 5V ±5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	MAX		
t_{RC}	Read Cycle Time	250		ns	
t_{CE}	CEB Access Time		250	ns	OEB = VIL
t_{AA}	Address Access Time		250	ns	CEB = OEB = VIL
t_{OE}	OEB Access Time		125	ns	CEB = VIL
t_{DF}	OEB or CEB High to Output Hi Z		130	ns	CEB OR OEB = VIL IO = ±3mA
t_{OH}	Output Hold from Address Change	0		ns	CEB = OEB =VIL (Note 1)
t_{OHZ}	OEB High to High Z Output	25		ns	IO = ±3mA

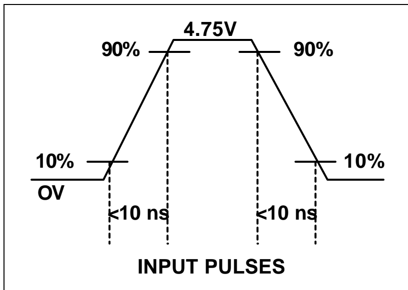
Note:

1. Verified by functional testing.

Read Cycle



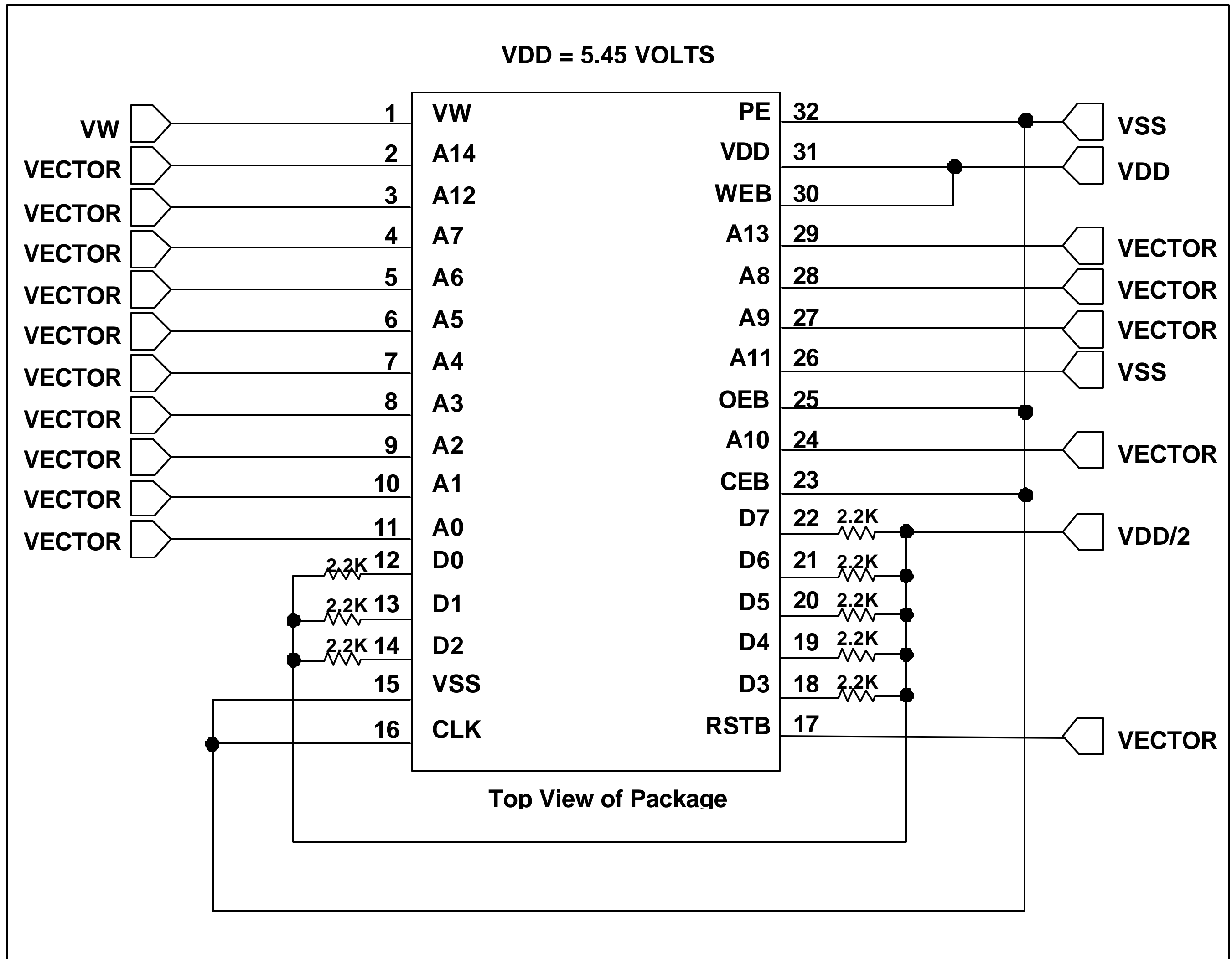
AC Test Loads and Input Waveforms



CAPACITANCE T_A = 25°C f = 1 MHz

Symbol	Parameter	MAX	Conditions
C_{IN}	Input Capacitance	5 pF	Vin = 0
C_{OUT}	External Load Capacitance	70 pF	AC Operations

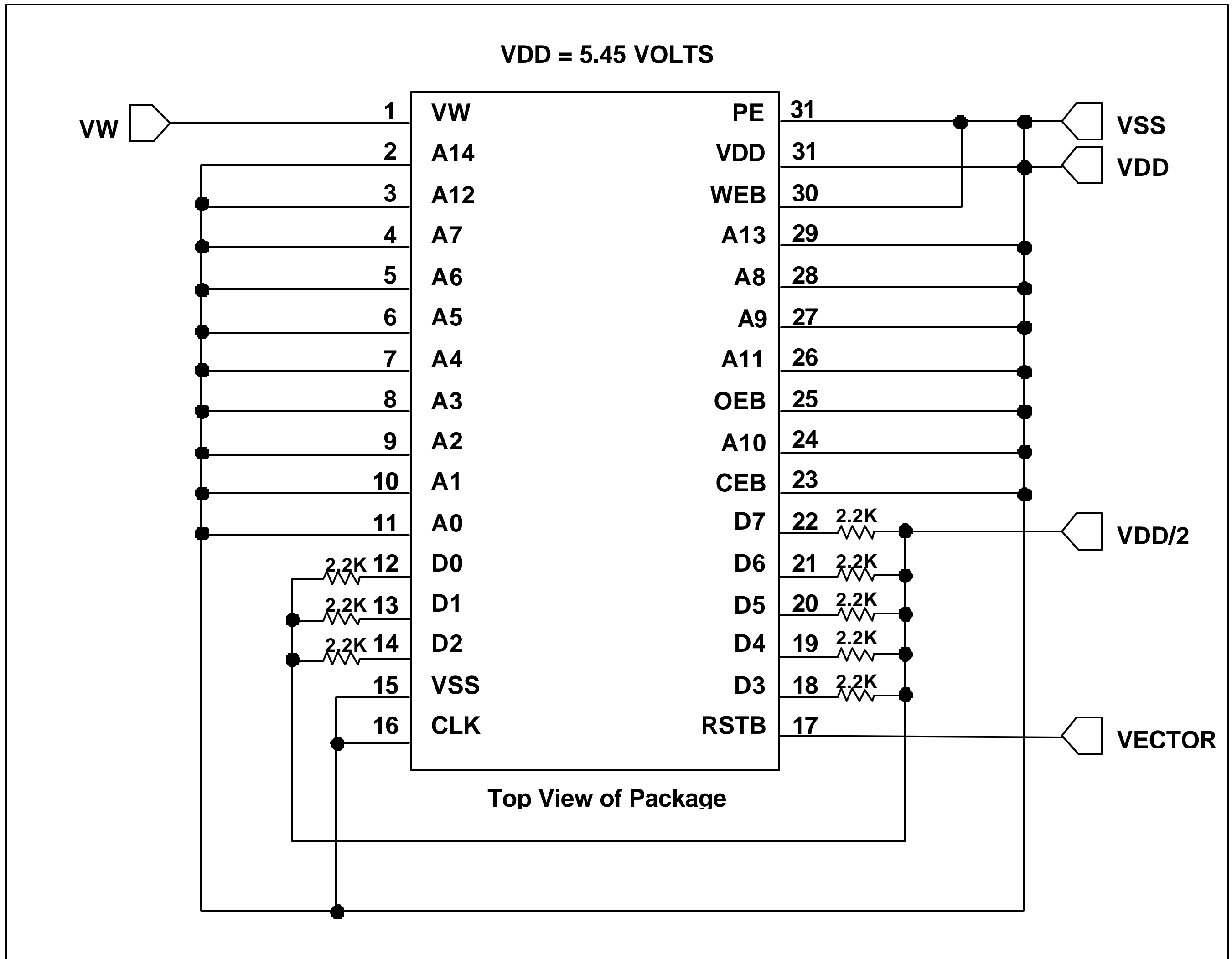
Dynamic Burn-in Circuit



Notes:

1. Incorporate isolation resistors (~ 3K ohm) at pins 2-11, 17, 24, and 26-29.
2. For Dynamic Burn-In
   VW = GND
   RSTB = GND

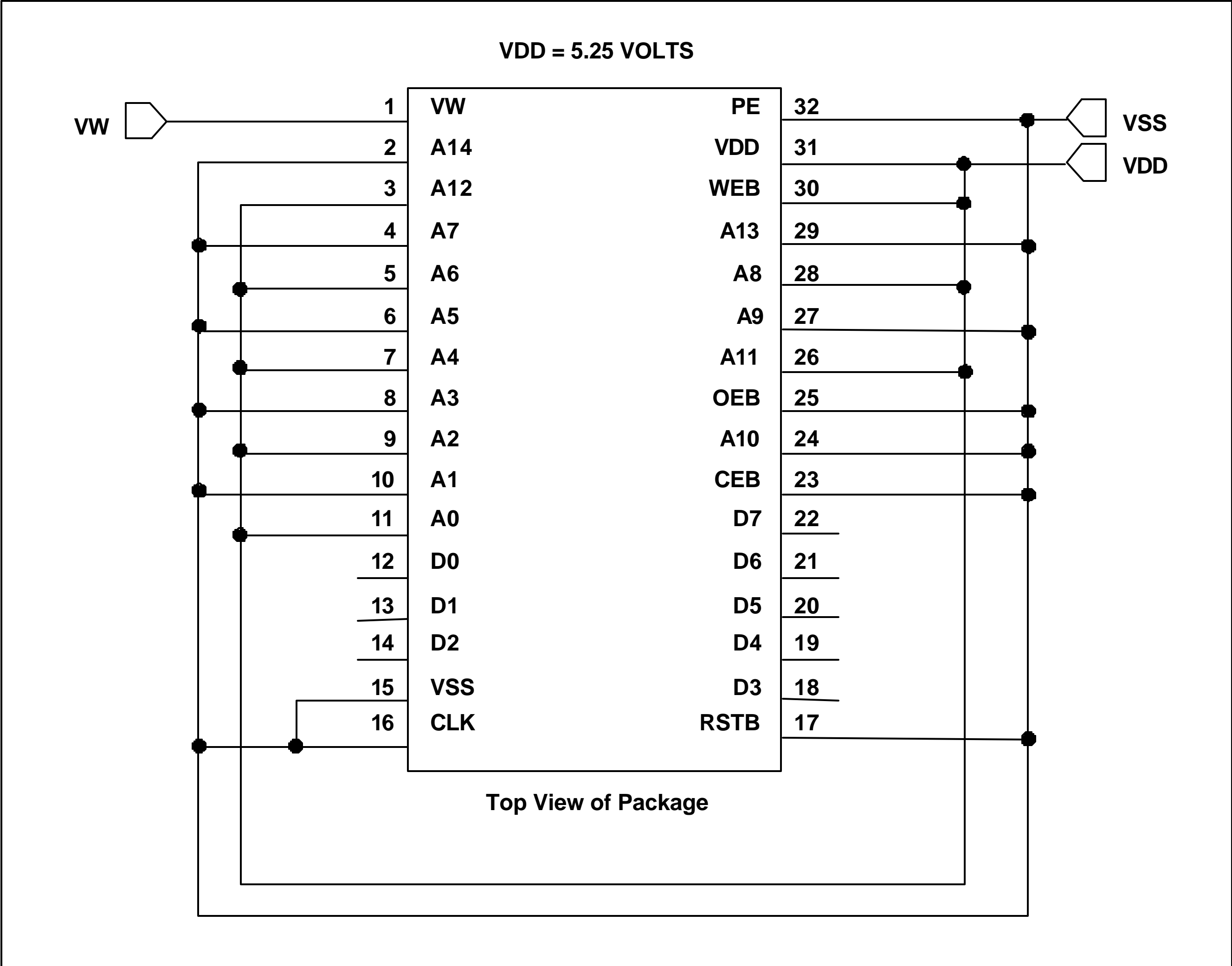
Static Burn-in Circuit



Notes:

1. Incorporate isolation resistors (~ 3K ohm) at pins 2-11, 17, 24, and 26-29. (Total of 16 resistors/device location).
2. VW = GND
3. RSTB = GND

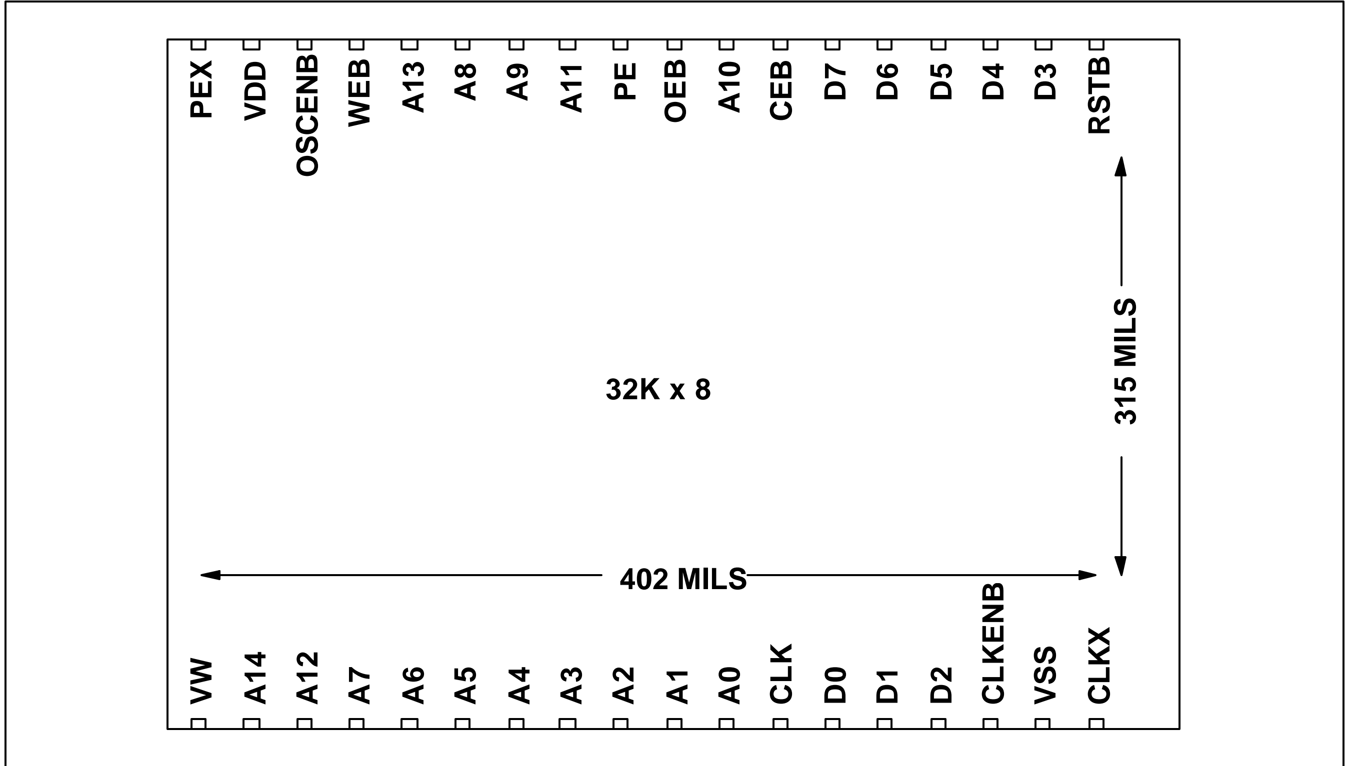
Radiation Bias Circuit



Notes:

1. VW = GND

W28C256 Die Information



CLKENB: An internal oscillator enable pin, has internal pullup to keep disabled.
CLKX: A redundant CLKIN pin. CLKIN and CLKX are internally connected.
PEX: A redundant PE pin. PE and PEX are internally connected.
OSCENB: Similar to CPEB on 64K. This will enable the on board charge pump and eliminate the need for VW (-5V). There is an internal pull down to keep the charge pump disabled, OSCENB is active hi.

32 Pin Flatpack